Si5351 – Modifying the Feedback Multisynth Dividers

Silicon Labs Timing Knowledge Base Article # 311668

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The equations to modify the feedback dividers are the same as for output Multisynth dividers (see KB article titled *Modifying Output Clock Frequencies on the Fly*, article #311538). However, any changes to the feedback Multisynth will require a PLL reset. PLLA and PLLB are reset by setting register 177 bits 5 and 7 respectively to 1.

$$Divider\ represented\ as\ a + \frac{b}{c}$$

$$\text{MSx\_P1} = 128 \times a + Floor\left(128 * \frac{b}{c}\right) - 512$$

$$\text{MSx\_P2} = 128 \times b - c \times Floor\left(128 * \frac{b}{c}\right)$$

$$\text{MSx\_P3} = c$$

Register 26. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P3[15:8]	**Multisynth NA Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLA Feedback MultiSynth divider.

Register 27. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P3[7:0]	**Multisynth NA Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLA Feedback MultiSynth divider.

Register 28. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Unused				Reserved		MSNA_P1[17:16]	
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function

7:4	Unused	**Unused.**
3:2	Reserved	**Reserved.** Leave as default, 0.
1:0	MSNA_P1[17:16]	**Multisynth NA Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLA Feedback MultiSynth divider.

Register 29. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P1[15:8]	**Multisynth NA Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLA Feedback MultiSynth divider.

Register 30. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P1[7:0]	**Multisynth NA Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLA Feedback MultiSynth divider.

Register 31. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P3[19:16]				MSNA_P2[19:16]			
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:4	MSNA_P3[19:16]	**Multisynth NA Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLA Feedback MultiSynth divider.
3:0	MSNA_P2[19:16]	**Multisynth NA Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLA Feedback MultiSynth divider.

Register 32. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0

Name	MSNA_P2[15:8]
Type	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P2[15:8]	**Multisynth NA Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLA Feedback MultiSynth divider.

Register 33. Multisynth NA Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNA_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNA_P2[7:0]	**Multisynth NA Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLA Feedback MultiSynth divider.

Register 34. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P3[15:8]	**Multisynth NB Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLB Feedback MultiSynth divider.

Register 35. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P3[7:0]	**Multisynth NB Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLB Feedback MultiSynth divider.

Register 36. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Unused				Reserved		MSNB_P1[17:16]	

Type	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Unused	**Unused.**
3:2	Reserved	**Reserved.** Leave as default, 0.
1:0	MSNB_P1[17:16]	**Multisynth NB Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLB Feedback MultiSynth divider.

Register 37. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P1[15:8]	**Multisynth NB Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLB Feedback MultiSynth divider.

Register 38. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P1[7:0]	**Multisynth NB Parameter 1.** This 18-bit number is an encoded representation of the integer part of the PLLB Feedback MultiSynth divider.

Register 39. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P3[19:16]				MSNB_P2[19:16]			
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:4	MSNB_P3[19:16]	**Multisynth NB Parameter 3.** This 20-bit number is an encoded representation of the denominator for the fractional part of the PLLB Feedback MultiSynth divider.
3:0	MSNB_P2[19:16]	**Multisynth NB Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLB Feedback MultiSynth divider.

Register 40. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P2[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P2[15:8]	**Multisynth NB Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLB Feedback MultiSynth divider.

Register 41. Multisynth NB Parameters

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSNB_P2[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSNB_P2[7:0]	**Multisynth NB Parameter 2.** This 20-bit number is an encoded representation of the numerator for the fractional part of the PLLB Feedback MultiSynth divider.