CRYSTAL SELECTION GUIDE FOR Si5350/51 DEVICES

1. Introduction

The Si5350/51 Any-Frequency CMOS Clock Generator + VCXO features an onboard crystal oscillator and VCXO that utilizes a standard, non-pullable 25/27 MHz crystal, PLLs, and MultiSynth fractional dividers to generate up to eight unique non-integer-related frequencies with exact frequency (0 ppm error). The Si5350/51 also features onboard crystal load capacitors ranging from 6 to 10 pF selectable through factory programming on the pin-controlled Si5350 or via an I^2C interface available on the Si5351.

This application note provides guidance on the selection of crystals that use the internal load capacitors or a combination of internal and external load capacitors and describes the operation of the crystal oscillator and the VCXO.

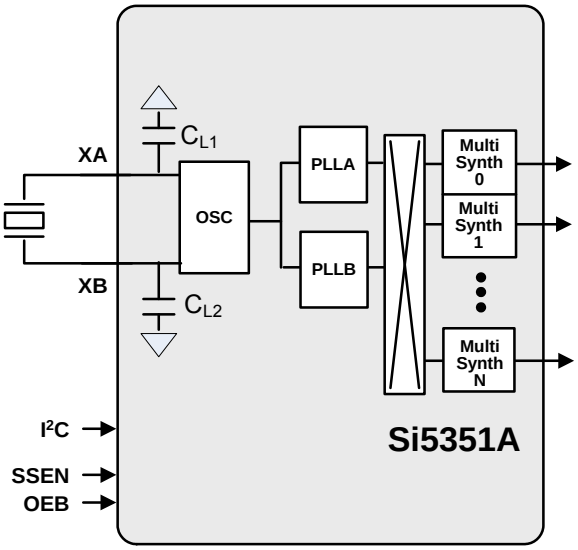


Figure 1. Si5351A Driven by a Standard, Non-Pullable Crystal

2. Crystal Selection, Load Capacitors, and Layout Guidelines

2.1. Crystal Selection and Load Capacitors

The Si5350/51 supports both 25 MHz and 27 MHz crystals and has integrated crystal load capacitors, eliminating the need for external components. Alternatively, the Si5350/51 can be configured to use a combination of internal and external load capacitors.

2.1.1. Internal Load Capacitors

Since the Si5350/51 has onboard load capacitors, it is recommended to select crystals with load capacitance specifications supported by the Si5350/51. For ease of use, Silicon Labs has qualified a number of crystals for use with the Si5350/51.

Table 1 lists the crystals that have been qualified for use with the Si5350/51. The Si5350/51, however, can also function with crystals that are not listed. In this case, select crystals with a load capacitance specification meeting the Si5350/51 data sheet specifications, with an ESR rating less than 150, and housed in a 5x7 mm^2 or smaller package. Crystals packaged in an HC-49 metal can are not recommended for use with the Si5350/51.

Table 1. Si5350/51 Qualified Crystals

MFR	PN	Freq (MHz)	C_L (pF)	Accuracy (ppm)	Stability over Temp (ppm)
Epson	FA-238 25.0000MB-K	25	10	±50	±30
Kyocera	CX3225SB25000D0FLJZ1	25	8	±10	±15
Kyocera	CX3225SB27000D0FLJZ1	27	8	±10	±15
NDK	NX3225GA-25.000M-STD-CRG-2	25	8	±20	±30
NDK	NX3225GA-27.000M-STD-CRG-2	27	8	±20	±30
TXC	7M-27.000MEEQ	27	10	±10	±10
Sunny	SP10115J6-25.000 MHz	25	10	±15	±30
Sunny	SP10115J6-27.000 MHz	27	10	±15	±30

2.1.2. External and Internal Load Capacitors

The Si5350/51 can use both internal and external load capacitors simultaneously to meet a crystal's load capacitor requirement. When using both internal and external load capacitors, it is recommended that external load capacitors of less than 2 pF and total load capacitance less than or equal to 12 pF be used to minimize additive jitter associated with larger external capacitors.

2.2. Layout Guidance

The Si5350/51's crystal oscillator is an analog circuit; so, layout of the crystal should follow analog rules. The following is a list of general crystal layout guidelines.

1. Since the total load capacitance is the summation of PCB trace capacitance and pin capacitance at the XA and XB pins, it is recommended that a crystal be placed as close to the Si5350/51 as possible to minimize parasitic capacitance.
2. Minimize trace lengths to less than 9 mm.
3. Clocks and frequently switched signals should not be routed close to the crystal.
4. Crystal traces should be protected with ground traces and guard rings.
5. Guard rings should not be connected to other ground connections on the PCB.
6. When two-layer PCBs are used, digital signals should not be routed on the opposite side of the PCB directly under the crystal.
7. It is recommended to fill the opposite side of the PCB under the crystal with a clean ground plane.

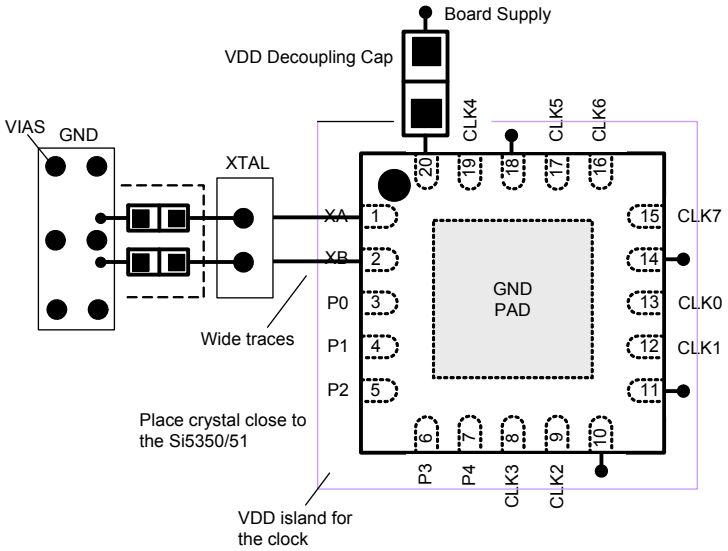


Figure 2. Si5350/51 Layout Example

3. Crystal Oscillator

3.1. Oscillator Model

The Si5350/51 crystal oscillator is based on a Pierce Oscillator architecture as shown Figure 3. The oscillator contains an Automatic Gain Control Circuit (AGC), which operates in high-gain and normal-gain modes. Upon startup, the AGC is configured in high-gain mode and the amplifier generates a large negative resistance (–R) to ensure crystal startup. Once a stable frequency of operation is achieved, the AGC is configured in normal gain mode, and (–R) is lowered to maintain oscillation.

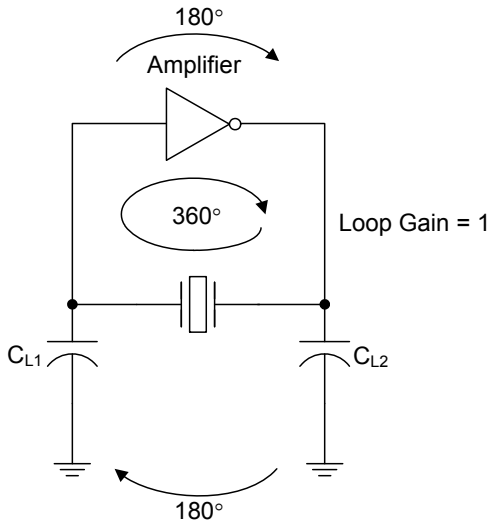


Figure 3. Si5350/51 Oscillator Circuit

When the crystal oscillator is in high-gain mode, the closed loop gain (G_{LP}) around the loop is greater than 1 to guarantee crystal start up. In normal gain mode, G_{LP} is reduced to 1 to maintain oscillation.

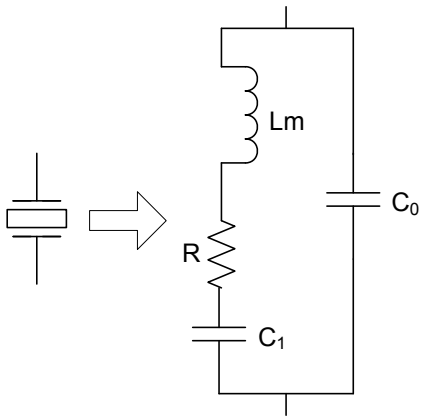
Table 2. Crystal Oscillators Modes

Mode	Gain	Loop Gain
Startup	High Gain, High (–R)	$G_{LP} \geq 1$
Sustained Oscillation	Normal Gain, Normal (–R)	$G_{LP} = 1$

3.2. Oscillator Accuracy

The Si5350/51 output accuracy depends on the reference clock, crystal, and mismatch between the external and internal load capacitance. Accuracy does not depend on the Si5350/51 PLLs since it is able to generate any combination of output frequencies exactly to (0 ppm) frequency synthesis error.

The generated output frequency accuracy can be modeled using a simple equivalent electrical circuit. The motional inductance and motional capacitance determine the resonant frequency.



Symbols:
Crystal Resistance: R
Motional Inductance/Capacitance: L_M, C_1
Packaging Capacitance: C_0

Figure 4. Equivalent Crystal Model

From this model, the frequency of the crystal oscillator can be modelled as Equation 1. Equation 1 accounts for the inaccuracy caused by the mismatched capacitor loading and takes into account factors including packaging capacitance and total load capacitance.

$$f_{OUTPUT} = f_{CRYSTAL}\left(1 - \frac{C_1}{2}\left(\frac{1}{C_0 + C_{SPEC}} + \frac{1}{C_0 + C_{CTL}}\right)\right)$$

Symbols:

Crystal Oscillator Frequency: f_{OUTPUT}

Crystal Frequency: $f_{CRYSTAL}$

Crystal Load Capacitance Specification: C_{SPEC}

Total Crystal Load Capacitance: C_{TL}

Package Capacitance: C_0

Motional Capacitance: C_1

Equation 1. Crystal Oscillator Frequency

Based on this equation, when the total capacitance is less than a crystal's load specification, the output frequency is less than the target frequency. In addition, when the total capacitance is greater than a crystal's load specification, the output frequency is greater than its target frequency. Table 3 summarizes the various cases of total load vs. accuracy.

Table 3. Crystal Accuracy vs. Load Capacitance

Case	Accuracy
$C_{SPEC} = C_{TL}$	0 ppm
$C_{SPEC} > C_{TL}$	–ppm
$C_{SPEC} < C_{TL}$	+ppm

The following example illustrates this relationship. Figure 5 summarizes the measured crystal frequency results when an Si5350/51 was tested with a 12 pF crystal. The load was varied, and the crystal frequency was determined. When the total crystal load was 12 pF, the generated frequency was 0 ppm; when the total crystal load was less than 12 pF, the generated frequency was greater than 0 ppm, and when the total crystal load was greater than 12 pF, the generated frequency was less than 0 ppm. Further, it is recommended that crystals with a total crystal load capacitance less than or equal 12 pF be used.

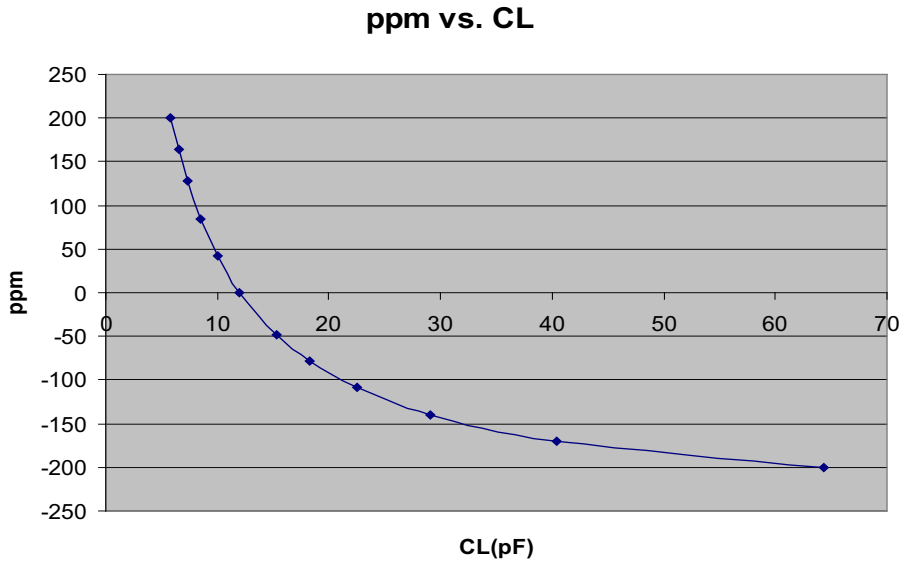


Figure 5. Crystal Driver Frequency vs. Crystal Load

3.3. Reactance

Electrically, a crystal is a series resonant circuit, and the reactance of the crystal is a function of its frequency. A crystal's reactance is 0 Ω at both the series resonant frequency (f_S) and parallel resonant frequency (f_P). f_S depends on C_1 and L_M, given by Equation 2.

$$f_s = \frac{1}{2\pi\sqrt{LmC_1}}$$

Symbols:

Series Resonance Frequency: F_S

Motional Inductance: L_M

Motional Capacitance: C_1

Equation 2. Series Resonant Frequency

F_P is like F_S, but F_P takes into account the packaging capacitance, C_0, and is given by Equation 3.

$$f_P = f_S\sqrt{1 + \frac{C_1}{(C_0 + C_L)}}, \text{ where } f_S = \frac{1}{2\pi\sqrt{L_M C_1}}$$

Symbols:

Parallel/Series Resonant Frequency: f_P, f_S

Motional Inductance/Capacitance: L_M, C_1

Packaging Capacitance: C_0

Equation 3. Parallel Resonant Frequency

As shown in Figure 6, negative reactance effectively looks inductive, and positive reactance effectively looks capacitive.

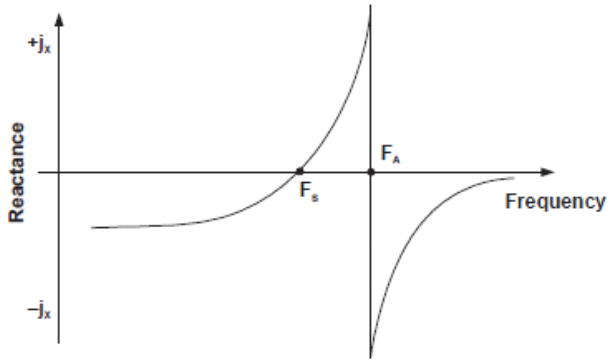


Figure 6. Crystal Effective Reactance

3.4. ESR Value

When selecting a crystal, a crystal's equivalent series resistance value (ESR) is an important parameter to consider. ESR depends on R_M, C_0, and C_L, where C_L is the required load capacitance of a crystal and is calculated by Equation 4. Note that the Si5350/51 can be used with crystals with an ESR greater than 150 Ω.

$$ESR = R_M\left(1 + \frac{C_0}{C_L}\right)^2$$

Symbols:

Electrical Series Resistance: ESR

Packaging Resistance: R_M

Packaging Capacitance: C_0

Specified Load Capacitance: C_L

Equation 4. Equivalent Series Resistance

ESR represents the loss of the crystal oscillator. Smaller crystals (especially crystals housed in SMD packages) tend to have larger ESR values. A higher ESR value represents higher loss. If the ESR value is too high, the crystal oscillator may fail to start, become unstable, or even stop oscillating. The (–R) of the Si5350/51's crystal oscillator is used to overcome the ESR of a crystal. (–R) of the Si5350/51 can be determined by adding a resistor in series with a crystal as show in Figure 7.

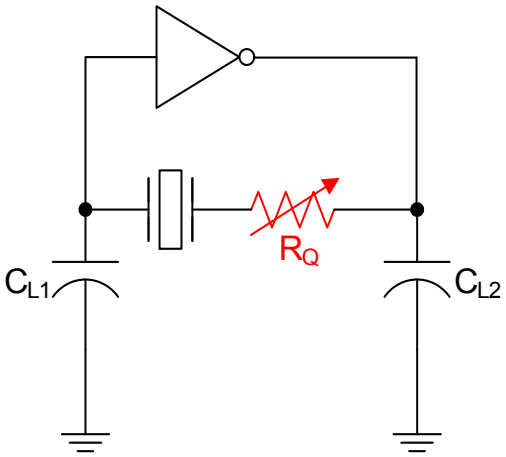


Figure 7. (–R) Test

In order to determine the (–R) of the crystal oscillator, the series resistance (R_Q) is slowly increased until the oscillator fails to start up or fails to sustain oscillation. R_Q can be realized with an SMD potentiometer. The (–R) test is performed by the startup and stop procedures described below.

3.4.1. Test 1: Startup Test Procedure

1. Place an SMD resistor (R_Q) in series with the crystal.
2. Power-on the device, and check if oscillation begins. Then, repeat the test by slowly incrementing the resistor value until the Si5350/51 fails to start.
3. The highest value resistor when the Si5350/51 fails to start is the startup value, R_Q.

3.4.2. Test 2: Stop Test Procedure

1. While the Si5350/51 is running, increase the resistor value until oscillation stops.
2. Once oscillation stops, reduce R_Q until oscillation starts.
3. The highest R_Q value with which the oscillator runs is the stop value.
4. The stop value should be equal to the startup value, R_Q.

Once R_Q is determined, the Safety Factor (SF) shown in Equation 5 determines whether the crystal driver has enough (–R) to start the crystal and sustain oscillation.

$$SF = \frac{R_Q + ESR}{ESR}$$

Symbols:

Safety: SF

Critical Resistance: R_Q

Electrical Series Resistance: ESR

Equation 5. Safety Factor Equation

An SF value of (SF ≥ 5) is needed to ensure stable oscillation. In addition, because the Si5350/51 crystal oscillator has an AGC, it is safe to operate the Si5350/51 with (SF >> 10). Table 4 summarizes the various ranges of SF values.

Table 4. Safety Factor Values

SF Value	Qualification
SF ≥ 5	Minimum Safe Value
SF >> 10	Very Safe Value

3.5. Negative Resistance

The (–R) was determined for the Si5350/51 using various crystals with different packaging capacitance (C_0). The data below illustrates the (–R) as a function of C_0.

3.5.1. CL = 6 pF

Table 5. R1, C0 Requirement—27 MHz Crystal (Safety Factor = 1)

Startup and Steady State – C0 (pF)	ESR (Ω)
5	337
4.5	385
4	445
3.5	517
3	606
2.5	716
2	852

Table 6. R1, C0 Requirement—25 MHz Crystal (Safety Factor = 1)

Startup and Steady State – C0 (pF)	ESR (Ω)
5	356
4.5	410
4	476
3.5	557
3	659
2.5	787
2	948

3.5.2. CL = 8 pF

Table 7. R1, C0 Requirement—27 MHz Crystal (Safety Factor = 1)

Startup and Steady State – C0 (pF)	ESR (Ω)
5	333
4.5	368
4	409
3.5	455
3	508
2.5	568
2	637

Table 8. R1, C0 Requirement—25 MHz Crystal (Safety Factor = 1)

Startup and Steady State – C0 (pF)	ESR (Ω)
5	367
4.5	408
4	456
3.5	510
3	573
2.5	646
2	730

3.5.3. CL = 10 pF

Table 9. R1, C0 Requirement—27 MHz Crystal (Safety Factor = 1)

Startup and Steady State – C0 (pF)	ESR (Ω)
5	288
4.5	311
4	336
3.5	365
3	396
2.5	430
2	468

Table 10. R1, C0 Requirement—25 MHz Crystal (Safety Factor = 1)

Startup and Steady State – C0 (pF)	ESR (Ω)
5	326
4.5	353
4	384
3.5	418
3	456
2.5	497
2	543

4. VCXO

The Si5350/51 VCXO is an advancement in VCXO technology because it modulates the PLL parameters instead of pulling a crystal to generate the VCXO pull curve. Since the Si5350/51's VCXO does not pull a crystal, the Si5350/51 eliminates the need for high-cost, custom pullable crystals and provides multiple benefits outlined in Table 11.

Table 11. Si5350/51 VCXOs vs Conventional VCXOs

Conventional VCXOs	Si5350/51 VCXO
High cost, custom pullable crystal	Standard, low cost, non-pullable crystal
Vactor-based non-linearity limits operating range	Highly linear range: 10–90 VDD
Potential crystal startup issues	Reliable startup and operation
Limited crystal sourcing options	Simplified crystal sources

With competing VCXOs, the following crystal parameters must be considered:

1. C_0/C_1 ratio
2. Max drive level
3. Mechanical third overtone and location of associated harmonic spurs

It has been determined that, if a crystal does not have an adequate C0/C1 ratio (for competitor's VCXO), undesirable results can be generated as shown in Figure 8. In contrast, the Si5350/51 makes use of standard, non-pullable, low-cost crystals; therefore, special consideration is not required. In addition, the Si5350/51 VCXO has been designed so that the performance of the pull curve does not vary with temperature, supply voltage, or the model of crystal used. Further, the VCXO pull curve can be generated directly from a clock signal on the Si535xC since the Si5350/51 does not pull a crystal like competing devices.

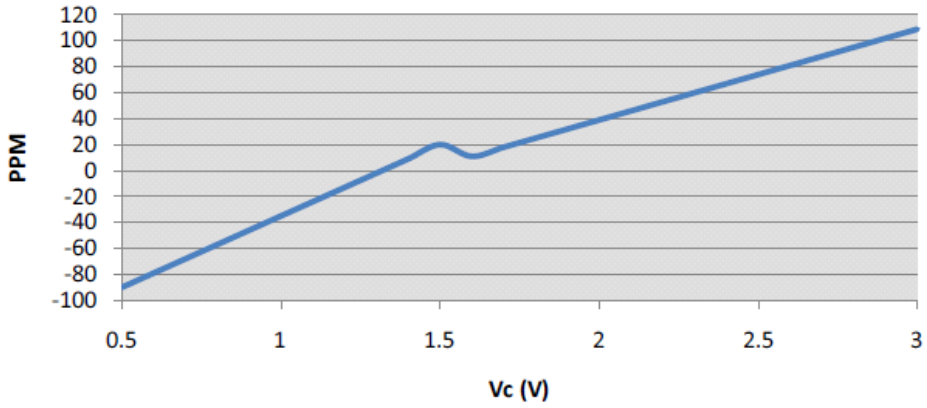


Figure 8. Competitors VCXO "Bump"

Further, because the Si5350/51 VCXO function changes the PLL parameters, the resulting VCXO transfer function is substantially more linear than competing devices which "pull" the crystal. Figure 9 shows the actual measured linearity of the Si5350/51 compared to the competition.

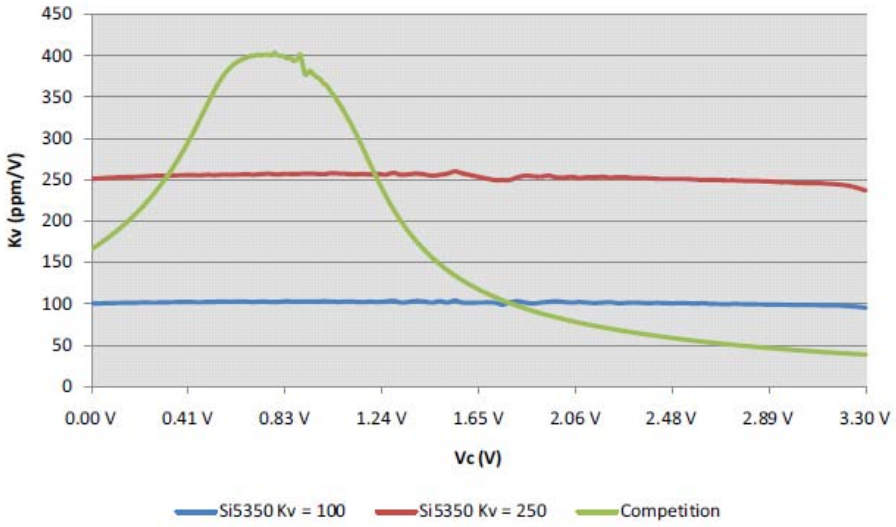


Figure 9. K_{VCO} Comparison of the Si5350/51 vs Competing Solutions

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}}$$

Equation 6. Equivalent Crystal Load Capacitance

4.1. Crystal Manufacturers

- http://www.eea.epson.com
- http://global.kyocera.com/index.html
- http://www.ndk.com/en
- http://www.txc.com.tw
- http://www.sunny-usa.com

Document Change List

Revision 0.1 to Revision 0.2

- Added "2.2. Layout Guidance" on page 3.
- Added "3.1. Oscillator Model" on page 4 to illustrate startup gain vs. sustained oscillation gain.
- Updated "3.2. Oscillator Accuracy" on page 5.
- Added "3.4. ESR Value" on page 7.

Revision 0.2 to Revision 0.3

- In “3.5. Negative Resistance” text, replaced “motional” with “packaging.”

NOTES:

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com